CLAIMS

What is claimed is:

1. An amplifier power detection circuit comprising:

an amplifier comprising plurality of amplifier stages coupled in series between an input node and an output node of the amplifier, wherein a signal path extends through the plurality of amplifier stages between the input node and the output node of the amplifier;

an interior node on the signal path within the amplifier located between, but not including, the input node and the output node; and

a power detector comprising an input coupled to the interior node, said power detector capable of sampling a first signal on the signal path at the interior node and outputting a second signal reflective of a power of the first signal.

2. The amplifier power detection circuit of claim 1 further comprising at least one intermediate said amplifier stage coupled along the signal path between a first said amplifier stage and a final said amplifier stage of the amplifier, wherein the interior node is between either the first amplifier stage and the at least one intermediate amplifier stage or between the at least one intermediate amplifier stage and the final amplifier stage.

3. The amplifier power detection circuit of claim 1 further comprising at least two intermediate said amplifier stages coupled between a first said amplifier stage and a final said amplifier stage of the amplifier, wherein the input of the power detector is coupled to the interior node between the at least two intermediate amplifier stages.

4. The amplifier power detection circuit of claim 1 further comprising a matching network coupled between respective ones of the plural amplifier stages, wherein the interior node comprises a node within the matching network.

5. The amplifier power detection circuit of claim 1, wherein the interior node is between the output of a first said amplifier stage and an output of a final said amplifier stage of the amplifier, exclusive of the output of the final amplifier stage.

6. The amplifier power detection circuit of claim 1, wherein the interior node is between the output of a first said amplifier stage and an input of a final said amplifier stage.

7. The amplifier power detection circuit of claim 6, further comprising a matching network between the first amplifier stage and the final amplifier stage, wherein the interior node is on the signal path within the matching network

8. The amplifier power detection circuit of claim 1 further comprising a matching network coupled between the final amplifier stage and the output node, wherein the internal node is within the matching network.

9. The amplifier power detection circuit of claim 1 wherein the power detector and the plurality of amplifier stages are entirely formed on a single integrated circuit.

10. The amplifier power detection circuit of claim 1, further comprising:

a second interior node on the signal path within the amplifier and located between, but not including, the input node and the output node of the amplifier;

a second power detector coupled to the second interior node, said second power detector capable of sampling the first signal at the second interior node and outputting a third signal reflective of a power of the first signal at the second interior node;

a first circuit coupled to receive the second and third signals, and capable of outputting a fourth signal derived from the second and third signals.

11. The amplifier power detection circuit of claim 10, wherein the first circuit comprises a summing circuit that sums the second and third signals to create the fourth signal.

12. The amplifier power detection circuit of claim 10, wherein the first circuit comprises a difference circuit the creates a difference between the second and third signals to create the fourth signal.

13. A method for detecting an output power of a multi-stage amplifier that comprises a plurality of amplifier stages, an input node, and an output node, with a signal path extending from the input node to the output node through the plurality of amplifier stages, the method comprising:

detecting a first signal at an interior node of the amplifier, said interior node being in the signal path within the multi-stage amplifier, exclusive of the input node and the output node; and

providing a second signal reflective of a power of the first signal at the interior node.

14. The method of claim 12 wherein the multi-stage amplifier includes at least a first said amplifier stage, an intermediate said amplifier stage, and a final said amplifier stage coupled in series on the signal path, and the interior node is between the first and intermediate amplifier stages, or the intermediate and final amplifier stages.

15. The method of claim 12, further comprising varying a reference voltage provided to a bias circuit that biases the amplifier based upon the second signal.

16. The method of claim 12, further comprising adjusting a degree of amplification of the first signal by the amplifier based on the second signal.

17. The method of claim 12, further comprising adjusting a magnitude of the first signal in response to the second signal at a point prior to the input node of the multi-stage amplifier.

18. The method of claim 12, wherein the interior node is between the output of a first said amplifier stage and an output of a final said amplifier stage, exclusive of the output of the final amplifier stage.

19. The method of claim 12, wherein the interior node is between the output of a first amplifier stage and an input of a final amplifier stage.

20. The method of claim 18, further comprising a matching network within the multi-stage amplifier between the first amplifier stage and the final amplifier stage, wherein the interior node is on the signal path within the matching network

21. The method of claim 12, further comprising:

detecting the first signal at a second interior node of the multi-stage amplifier, said second interior node being on the signal path within the multi-stage amplifier, exclusive of the input node and the output node;

providing a third signal reflective of a power of the first signal at the second interior node; and

using the second and third signals to create a fourth signal.

22. The method of claim 20, wherein in summing the second and third signals, a greater weight is given to one or the other of the second and third signals.

23. A wireless communications device comprising:

a processor;

an antenna;

a signal path between the processor and the antenna;

an amplifier comprising a plurality of amplifier stages in the signal path between the processor and the antenna, said amplifier including an interior node in the signal path between, and exclusive of, an input node of the amplifier that receives a first signal on the signal path and an output node of the amplifier from which the first signal goes to the antenna;

a power detector having an input coupled to the interior node and an output coupled to the processor,

wherein the power detector is operable to detect the first signal at the interior node and to provide a second signal to the processor reflective of a power of the first signal at the interior

node, and the processor is operable to adjust an amplitude of the first signal in response to the second signal.

24. The wireless communications device of claim 22, wherein the processor is coupled to the amplifier, and the processor operates to adjust an amplitude of the first signal by adjusting an amount of amplification of the first signal by the amplifier.

25. The wireless communications device of claim 22, wherein the processor operates to adjust the amplitude of the first signal by varying a reference voltage provided to a bias circuit that biases the amplifier.

26. The wireless communications device of claim 22, wherein the processor is coupled to a preamplifier in the signal path between the processor and the input node of the amplifier, and the processor operates to adjust the amplitude of the first signal by adjusting an amount of amplification of the first signal by the preamplifier prior to the signal reaching the input node of the amplifier.

27. The wireless communications device of claim 22, wherein the amplifier includes at least a first said amplifier stage and a final said amplifier stage coupled in series on the the signal path, and the interior node is between the an output of the first amplifier stage and an input of the final amplifier stage.

28. The wireless communications device of claim 22 wherein the amplifier includes at least a first said amplifier stage, an intermediate said amplifier stage, and a final said amplifier stage coupled in series on the signal path, and the interior node is between the first and intermediate amplifier stages, or the intermediate and final amplifier stages.

29. The wireless communications device of claim 22, wherein the interior node is within a matching network that is disposed within the amplifier on the signal path between a first said amplifier stage and a final said amplifier stage of the amplifier.

30. The wireless communication device of claim 22 wherein the power detector and the amplifier are entirely formed on a single integrated circuit.

31. A wireless communications device, comprising:

a processor;

an antenna;

a signal path between the processor and the antenna;

an amplifier comprising a plurality of amplifier stages in the signal path between the processor and the antenna, said amplifier including a plurality of interior nodes in the signal path between, and exclusive of, an input node of the amplifier that receives a first signal on the signal path and an output node of the amplifier from which the first signal goes to the antenna;

a power detector comprising a plurality of inputs and an output, wherein each said the input is coupled to a separate one of the interior nodes, the power detector is operable to detect the first signal at the respective interior node, and the power detector is operable to output a second signal that reflects a power of the first signal at the plurality of interior nodes, and

wherein the processor is operable to adjust an amplitude of the first signal in response to the second signal.

32. The wireless communications device of claim 30, wherein the processor is coupled to the amplifier, and the processor operates to adjust an amplitude of the first signal by adjusting an amount of amplification of the first signal by the amplifier.

33. The wireless communications device of claim 30, wherein the processor operates to adjust the amplitude of the first signal by varying a reference voltage provided to a bias circuit that biases the amplifier.

34. The wireless communications device of claim 30, wherein the processor is coupled to a preamplifier in the signal path between the processor and the input node of the amplifier, and the processor operates to adjust the amplitude of the first signal by adjusting an amount of amplification of the first signal by the preamplifier prior to the signal reaching the input node of the amplifier.

35. The wireless communications device of claim 30, wherein the amplifier includes at least a first said amplifier stage and a final said amplifier stage coupled in series on the signal path, and at least one detected said interior node is between an output of the first amplifier stage and an input of the final amplifier stage.

36. The wireless communications device of claim 30 wherein the amplifier includes at least a first said amplifier stage, an intermediate said amplifier stage, and a final said amplifier stage coupled in series on the signal path, and one said detected interior node is between the first and intermediate amplifier stages, and another said detected interior node is between intermediate and final amplifier stages.

37. The wireless communications device of claim 30, wherein at least one said interior node is within a matching network that is disposed within the amplifier on the signal path between a first said amplifier stage and a final said amplifier stage of the amplifier.

38. The wireless communications device of claim 30, wherein the second signal is a sum of respective signals derived from respective said interior node.